IDEC Chip Design Contest

A Low-Power CNN-Based Face Recognition Processor with Face Alignment for Mobile User Identification

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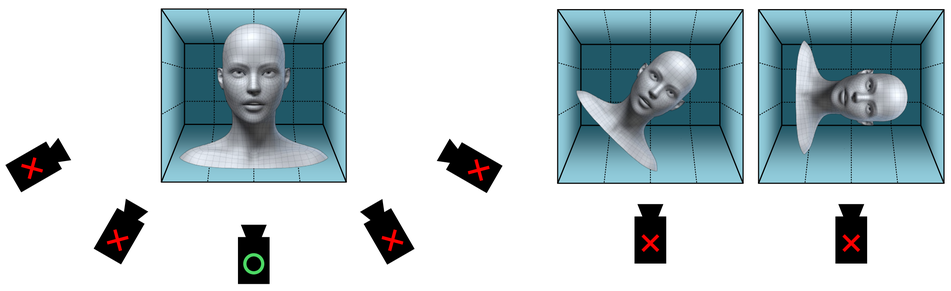
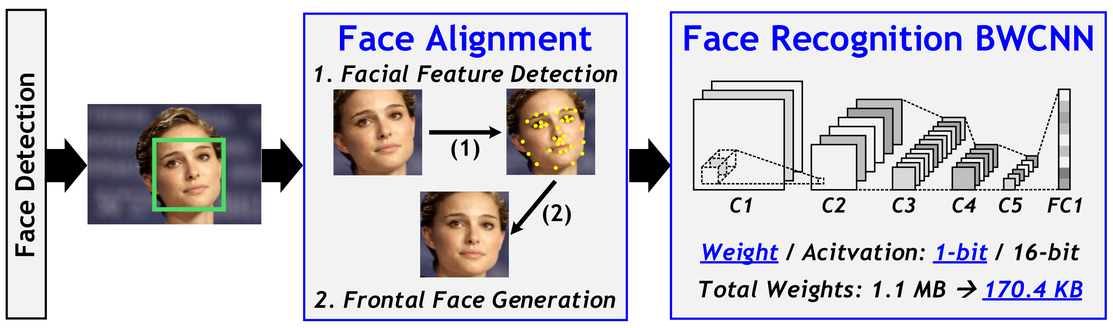
Motivation

- Face Recognition w/ Pose Variance

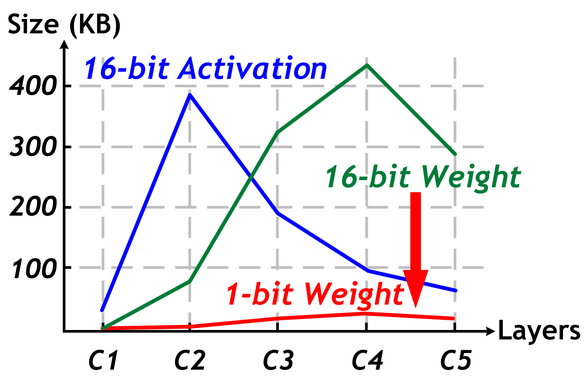


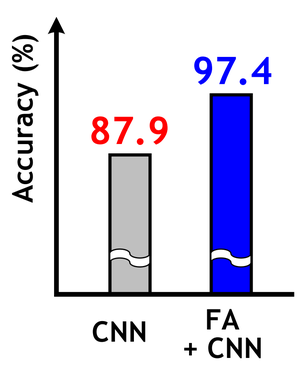
➔ CNN recognition fails from different position / angle!

- Proposed Face Recognition System



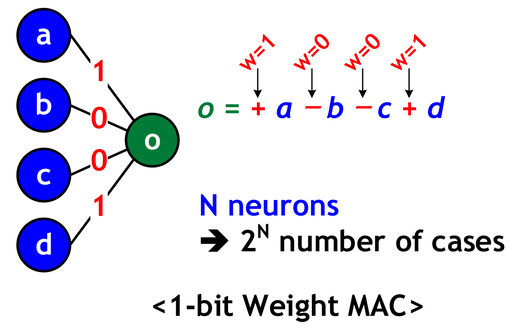
- BWCNN Data Pattern

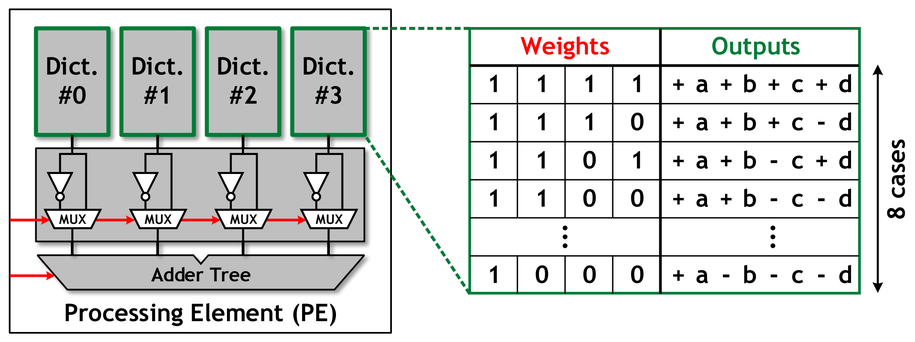




Binary Convolution Core

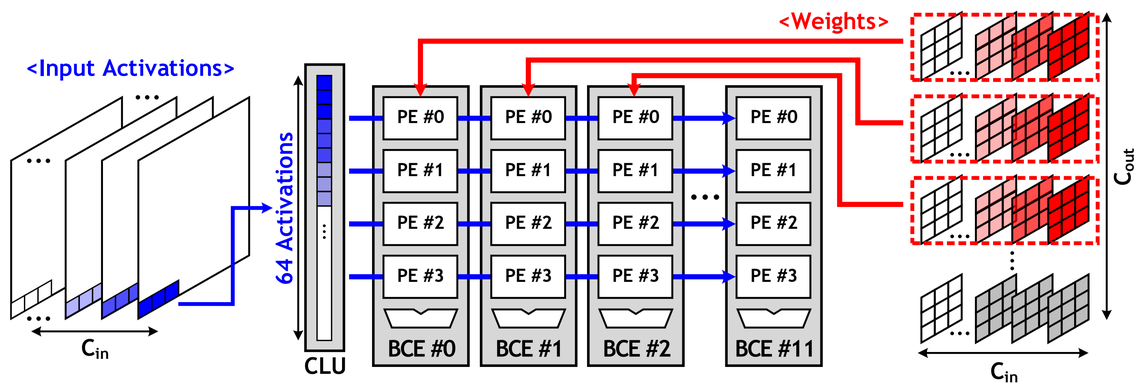
- Dictionary-Based Processing Element (PE)





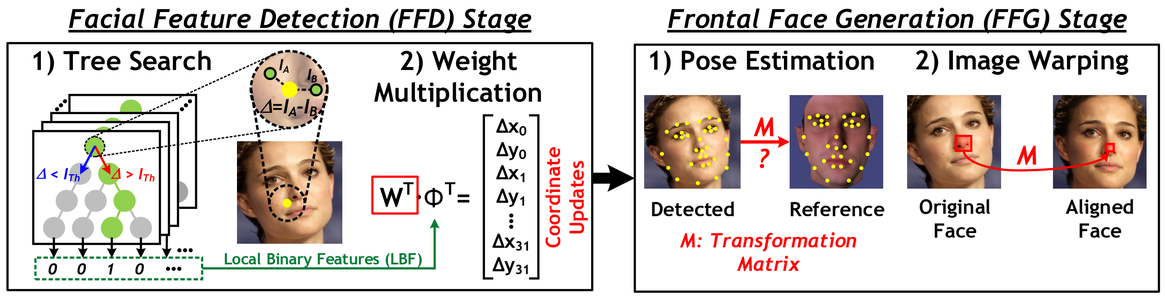
➔ 54% energy reduction compared to conventional MAC unit

- CNN Mapping to Binary Convolution Core

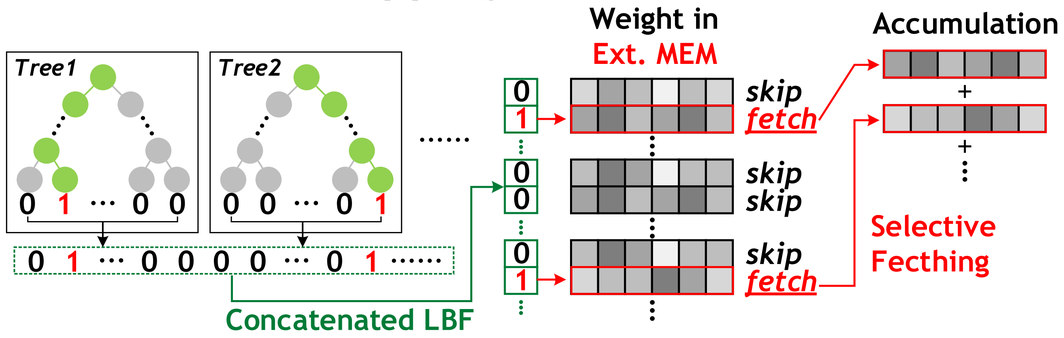


Face Alignment Core

- Face Alignment Algorithm

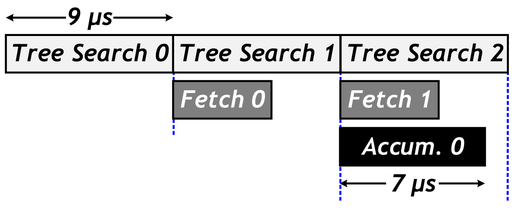


- Zero-Aware Skipping



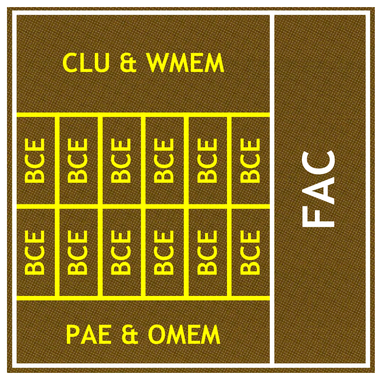
➔ 93.8% external memory access reduction

- Tree-Level Pipeline



➔ 60% throughput increase

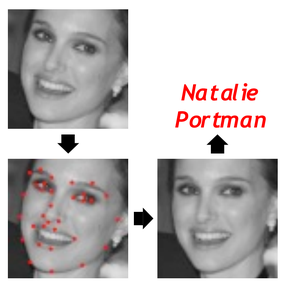
Verification



	Specification
Technology	65 nm Logic CMOS
Die Area	1784×1784 μm²
SRAM	56 KB
Supply Voltage	0.66 V ~ 1.2 V
Frequency	5 MHz ~ 100 MHz
FR Framerate	1 fps
FR Power Consumption	0.2 mW @(0.66 V, 5 MHz)
CNN Power Efficiency	13.6 TOPS/W @(0.66 V, 5 MHz)

- Face Recognition BWCNN Performance

Layers	Kernel Size	Input Size	In/Out Channels	Latency [ms]
Conv 1	5×5	128	1/48	23
Conv 2	3×3	64	48/96	81
Conv 3	3×3	32	96/192	58
Conv 4	3×3	16	192/128	19
Conv 5	3×3	16	128/128	12
FC1	·	8	128/256	1
Total	Avg. Power		0.53 mW	196



- Verification System